1. (Currently Amended) A data transfer method for transferring data between two processing systems, wherein said two processing systems operate independently, said method comprising:

receiving data from a [first] physical layer processing system;

storing the received data into a first memory device; and

executing a single program instruction on [an associated] a media access control layer processor to directly transfer at least a portion of the stored data to a [second] main memory device.

2. (Currently Amended) A data transfer method according to claim 1, wherein said method further comprises:

transferring at least a portion of the data stored in said [second] main memory device to a [third] host memory device, upstream of a host processor, wherein said [second processing system operates upon] media access control layer processor formats the data stored in said [third] host memory device using a host protocol.

3. (Original) A data transfer method according to claim 1, wherein said first memory device is a FIFO memory device.

4. (Currently Amended) A data transfer method according to claim [1] 2, wherein said [third] host memory device is a FIFO memory device.

5. (Original) A data transfer method according to claim 1, wherein method further comprises byte-aligning the data stored in said first memory device.

6. (Currently Amended) A data transfer method for transferring data between two processing systems, wherein said two processing systems operate independently, said method comprising:

receiving data from a [first] physical layer processing system;

storing the received data into a first memory device;

transferring a header portion and a data portion of the stored data to a [second] main memory device; and

executing a single program instruction on [an associated] a media access control layer processor to store [at least a] the data portion of the data stored in the [second] main memory device to a [third] host memory device upstream of a host processor.

7. (Currently Amended) A data transfer method according to claim 6, wherein said [second] media access control layer processing system [operates upon] formats the data stored in said [third] host memory device using a host protocol.

8. (Original) A data transfer method according to claim 6, wherein said first memory device is a FIFO memory device.

9. (Currently Amended) A data transfer method according to claim [6] 7, wherein said [third] host memory device is a FIFO memory device.

10. (Currently Amended) A system for transferring data between two processing systems, wherein said two processing systems operate independently, said system comprising:

means for receiving data from a [first] physical layer processing means;

means for storing the received data into a first memory means; and

executing a single program instruction on [an associated] a media access control layer processing means to directly transfer at least a portion of the stored data to a [second] main memory means.

11. (Currently Amended) A system according to claim 10, wherein said system further comprises:

means for transferring at least a portion of the data stored in said [second] main memory means to a [third] host memory means, upstream of a host processor, wherein said [second processing means operates upon] media access control layer processor formats the data stored in said [third] host memory means using a host protocol.

12. (Original) A system according to claim 10, wherein said first memory means is a FIFO memory device.

13. (Currently Amended) A system according to claim [10] 11, wherein said [third] host memory means is a FIFO memory device.

14. (Original) A system according to claim 10, wherein system further comprises means for byte-aligning the data stored in said first memory means.

15. (Currently Amended) A system for transferring data between two processing systems, wherein said two processing systems operate independently, said system comprising:

means for receiving data from a [first] physical layer processing means;

means for storing the received data into a first memory means;

means for transferring a header portion and a data portion of the stored data to a [second] main memory means; and

means for executing a single program instruction on [an associated] a media access control layer processor means to directly store [at least a] the data portion of the data stored in the [second] main memory means to a [third] host memory means upstream of a host processor.

16. (Currently Amended) A system according to claim 15, wherein said [second] media access control layer processing means [operates upon] formats the data stored in said [third] host memory means using a host protocol.

17. (Original) A system according to claim 15, wherein said first memory means is a FIFO memory device.

18. (Currently Amended) A system according to claim [15] 16, wherein said [third] host memory means is a FIFO memory device.

19. (Currently Amended) A system for transferring data between two processing systems, wherein said two processing systems operate independently, said system comprising:

a first memory device for storing data received from a [first] physical layer processing system; and

[an associated] a media access control layer processing device for executing a single program instruction to directly transfer[s] at least a portion of the stored data to a [second] main memory device.

20. (Currently Amended) A system according to claim 19, wherein said system further comprises hardware logic for transferring at least a portion of the data stored in said [second] main memory device to a [third] host memory device, upstream of a host processor, wherein [a second] the media access control layer processing system [operates upon] formats the data stored in said [third] host memory device using a host protocol.

21. (Original) A system according to claim 19, wherein said first memory device is a FIFO memory.

22. (Currently Amended) A system according to claim [19] 20, wherein said [third] host memory device is a FIFO memory.

23. (Original) A system according to claim 19, wherein said first memory device byte-aligns the data stored therein.

24. (Currently Amended) A system for transferring data between two processing systems, wherein said two processing systems operate independently, said system comprising:

a first memory device for storing data received from a [first] physical layer processing system;

a [second] main memory device for receiving a header portion and a data portion of the data stored in the first memory device; and

[an associated] a media access control layer processor for executing a single memory read instruction to directly transfer [at least a] the data portion of the data stored in the [second] main memory device to a [third] host memory device upstream of a host processor.

25. (Currently Amended) A system according to claim 24, wherein [said system further comprises a second processing system for operating upon] the media access control layer formats the data stored in said [third] host memory device using a host protocol.

26. (Original) A system according to claim 24, wherein said first memory device is a FIFO memory.

27. (Currently Amended) A system according to claim [24] 25, wherein said [third] host memory device is a FIFO memory.

28. (Currently Amended) A data transfer method for transferring data between two processing systems, wherein said two processing systems operate independently, said method comprising:

receiving a data packet from a [first] physical layer processing system, wherein said data packet includes a header portion and a data portion;

storing the received data packet into a first memory device;

directly transferring the data portion of the data packet from the first memory device to a [third] host memory device; and

executing at least one program instruction on an associated processor to transfer the header portion to a [second] main memory device.

29. (Currently Amended) A data transfer method according to claim 28, wherein a [second] media access control layer processing system [operates upon] formats the data portion stored in said [third] host memory device using a host protocol.

30. (Original) A data transfer method according to claim 28, wherein said first memory device is a FIFO memory device.

31. (Currently Amended) A data transfer method according to claim [28] 29, wherein said [third] host memory device is a FIFO memory device.

32. (Currently Amended) A system for transferring data between two processing systems, wherein said two processing systems operate independently, said system comprising:

means for receiving a data packet from a [first means for processing] physical layer processor, wherein said data packet includes a header portion and a data portion;

means for storing the received data packet into a first memory means;

means for transferring the data portion to a [third] host memory means; and

means for executing at least one program instruction on [an associated] a media access control layer processor to directly transfer the header portion to a [second] main memory means.

33. (Currently Amended) A system according to claim 32, wherein a [second means for processing operates upon] the media access control layer processor formats the data portion stored in said [third] host memory means using a host protocol.

34. (Original) A system according to claim 32, wherein said first memory means is a FIFO memory device.

35. (Currently Amended) A system according to claim [32] 33, wherein said [third] host memory means is a FIFO memory device.

36. (Currently Amended) A system for transferring data between two processing systems, wherein said two processing systems operate independently, said system comprising:

a first memory device for storing a data packet received from a [first] physical layer processing system, wherein said data packet includes a header portion and a data portion;

[an associated] a media access control layer processor for executing at least one program instruction on to directly transfer the header portion from the first memory device to a [second] main memory device; and

hardware logic enabled by [the associated] media access control layer processor to transfer the data portion from the first memory device to a [third] host memory device upstream of a host processor.

37. (Currently Amended) A system according to claim 36, wherein [said system further comprises a second processing system for operating upon] the media access control layer processor formats the data stored in said [third] host memory device using a host protocol.

38. (Original) A system according to claim 36, wherein said first memory device is a FIFO memory.

39. (Currently Amended) A system according to claim [36] 37, wherein said [third] host memory device is a FIFO memory.

40. (Currently Amended) A data processing system comprising:

a physical layer processor for transferring data to a memory location identified by an address stored in an address pointer register;

a FIFO memory for storing data; and

a first memory for storing data at a plurality of memory locations, each memory location identified by an address,

wherein the physical layer processor receives an instruction to transfer data directly from the FIFO memory to a memory location of the first memory identified by the address stored in the address pointer register, and automatically increments the address stored in the address pointer register to identify another memory location of the first memory, said instruction having a first parameter identifying the address pointer register, and a second parameter identifying the first memory.

41. (Currently Amended) A data processing system comprising:

a physical layer processor for transferring data from a memory location identified by an address stored in an address pointer register;

a first memory for storing data at a plurality of memory locations, each memory location identified by an address; and

a FIFO memory for storing data,

wherein the physical layer processor receives an instruction to transfer data directly from a memory location of the first memory identified by the address stored in the address pointer register to the FIFO memory, and automatically increments the address stored in the address pointer register to identify another memory location of the first memory, said instruction having a

first parameter identifying the address pointer register, and a second parameter identifying the FIFO memory.